

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal.

2. The semiconductor integrated circuit according to claim 1, wherein the gate of each transistor has a gate length and a gate width, the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is about three times or less than the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors.

3. The semiconductor integrated circuit according to claim 1, wherein the gate of each transistor has a gate length and a gate width, and the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors.

4. The semiconductor integrated circuit according to claim 1, wherein each transistor has a gain constant, and the gain constant of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the gain constant of the other one of the transistors in the pair of the series-connected MOS transistors.

5. The semiconductor integrated circuit according to claim 1, wherein each transistor has a channel modulation constant, and the channel modulation constant of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the channel modulation constant of the other one of the transistors in the pair of the series-connected MOS transistors.

6. The semiconductor integrated circuit according to claim 1, wherein the differential amplification circuit is connected between the first power supply and the second power supply.

7. The semiconductor integrated circuit according to claim 1, wherein the first to fourth MOS transistors each include a source and a back gate, which is connected to the

source.

8. The semiconductor integrated circuit according to claim 1, wherein the differential amplification circuit
5 includes a plurality of MOS transistors, each having a gate provided with a predetermined gate voltage capacity, the semiconductor device further comprising:

10 a fifth MOS transistor connected between the differential amplification circuit and the node connecting the first and second MOS transistors; and

a sixth MOS transistor connected between the differential amplification circuit and the node connecting the third and fourth MOS transistors, the fifth and sixth MOS transistors each having a gate to which voltage less
15 than the gate voltage capacity of each MOS transistor in the differential amplification circuit is applied.

9. The semiconductor integrated circuit according to claim 1, wherein the level conversion circuit includes:

20 a fifth MOS transistor having a gate for receiving a current restriction signal, a source connected to one of the first and second power supplies, and a drain connected to the gates of the first and fourth MOS transistors;

25 a sixth MOS transistor having a gate for receiving the current restriction signal, a source connected to one of the first and second power supplies, and a drain connected to the gates of the second and third MOS transistors.

10. The semiconductor integrated circuit according to claim 9, wherein the level conversion circuit includes:

a seventh MOS transistor, connected to one of the first and second power supplies, for fixing voltage to a predetermined value at the node connecting the first MOS

transistor and the second MOS transistor; and

an eighth MOS transistor, connected to one of the first and second power supplies, for fixing voltage to a predetermined value at the node connecting the third MOS transistor and the fourth MOS transistor.

11. The semiconductor integrated circuit according to claim 1, wherein the first to fourth MOS transistors are each N-type conduction transistors, and potential at one of the first and second power supplies is lower than potential at the other one of the first and second power supplies, the level conversion circuit including:

an N-type fifth MOS transistor having a gate for receiving a current restriction signal, a source connected to the one of the first and second power supplies at which the potential is lower, and a drain connected to the gates of the first and fourth MOS transistors; and

an N-type sixth MOS transistor having a gate for receiving the current restriction signal, a source connected to the one of the first and second power supplies at which the potential is lower, and a drain connected to the gates of the second and third MOS transistors.

12. The semiconductor integrated circuit according to claim 1, wherein the first to fourth MOS transistors are each P-type conduction transistors, and potential at one of the first and second power supplies is greater than potential at the other one of the first and second power supplies, the level conversion circuit including:

a P-type fifth MOS transistor having a gate for receiving a current restriction signal, a source connected to the one of the first and second power supplies at which the potential is greater, and a drain connected to the gates

of the first and fourth MOS transistors; and

a P-type sixth MOS transistor having a gate for receiving the current restriction signal, a source connected to the one of the first and second power supplies at which the potential is greater, and a drain connected to the gates of the second and third MOS transistors.

13. The semiconductor integrated circuit according to claim 1, wherein the differential amplification circuit includes a plurality of MOS transistors, each provided with a predetermined gate voltage capacity, the first to fourth MOS transistors of the level conversion circuit each being provided with a gate voltage capacity that is greater than the gate voltage capacity of each MOS transistor in the differential amplification circuit.

14. The semiconductor integrated circuit according to claim 1, wherein potential at one of the first and second power supplies is greater than potential at the other one of the first and second power supplies, and the differential amplification circuit is connected to the one of the first and second power supplies at which the potential is greater;

wherein the differential amplification circuit includes a plurality of MOS transistors, each provided with a predetermined gate voltage capacity, the first to fourth MOS transistors of the level conversion circuit each being provided with a gate voltage capacity that is greater than the gate voltage capacity of each MOS transistor in the differential amplification circuit; and

wherein the level conversion circuit receives an input signal having voltage greater than the greater one of the potentials at the first and second power supplies.

15. A semiconductor integrated circuit comprising:

a level conversion circuit having a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply, the level conversion circuit generating a first output signal from a node connecting the first and second MOS transistors and a second output signal from a node connecting the third and fourth transistors; and

a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit,

wherein the gate of each transistor has a gate length and a gate width, the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is about three times or less than the ratio between the gate length and the gate width of the other one of the transistors in each pair of the series-connected MOS transistors.

16. The semiconductor integrated circuit according to claim 15, wherein the first and fourth MOS transistors each receive a first input signal, and the second and third MOS transistors each receive a second input signal having a phase inverted from the phase of the first input signal.

17. A level conversion circuit for shifting voltage levels of a first input signal and a second input signal to generate an output signal, the level conversion circuit

comprising:

a pair of transistors including a first MOS transistor and a second MOS transistor, connected in series between a first power supply and a second power supply, and a further
5 pair of transistors including a third MOS transistor and a fourth MOS transistor, connected in series between the first power supply and the second power supply,

wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second
10 and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase of the first input signal.

18. The level conversion circuit according to claim
15 17, wherein the gate of each transistor has a gate length and a gate width, and the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is about three times or less than the ratio between the gate length and the gate
20 width of the other one of the transistors in the pair of the series-connected MOS transistors.

19. The level conversion circuit according to claim
25 17, wherein the gate of each transistor has a gate length and a gate width, and the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-
30 connected MOS transistors.

20. The level conversion circuit according to claim
17, wherein each transistor has a gain constant, and the

gain constant of one of the transistors in each pair of the series-connected MOS transistors is substantially the same as the gain constant of the other one of the transistors in the pair of the series-connected MOS transistors.

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